

## FEATURES

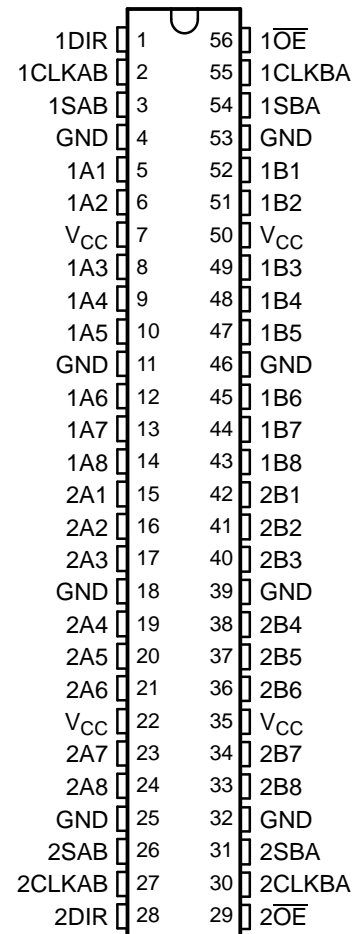
- Member of the Texas Instruments Widebus™ Family
- Operates From 1.65 V to 3.6 V
- Inputs Accept Voltages to 5.5 V
- Max  $t_{pd}$  of 5.7 ns at 3.3 V
- Typical  $V_{OLP}$  (Output Ground Bounce) <0.8 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot) >2 V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Supports Mixed-Mode Signal Operation on All Ports (5-V Input/Output Voltage With 3.3-V  $V_{CC}$ )
- $I_{off}$  Supports Partial-Power-Down Mode Operation
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Latch-Up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

## DESCRIPTION/ORDERING INFORMATION

This 16-bit bus transceiver and register is designed for 1.65-V to 3.6-V  $V_{CC}$  operation.

The SN74LVCH16646A can be used as two 8-bit transceivers or one 16-bit transceiver. The device consists of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers.

DGG, DGV, OR DL PACKAGE  
(TOP VIEW)



## ORDERING INFORMATION

| $T_A$         | PACKAGE <sup>(1)</sup> |               | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---------------|------------------------|---------------|-----------------------|------------------|
| –40°C to 85°C | SSOP – DL              | Tube          | SN74LVCH16646ADL      | LVCH16646A       |
|               |                        | Tape and reel | SN74LVCH16646ADLR     |                  |
|               | TSSOP – DGG            | Tape and reel | SN74LVCH16646ADGGR    | LVCH16646A       |
|               | TVSOP – DGV            | Tape and reel | SN74LVCH16646ADGVR    | LDH646A          |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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**SN74LVCH16646A**  
**16-BIT BUS TRANSCEIVER AND REGISTER**  
**WITH 3-STATE OUTPUTS**

SCAS318K–NOVEMBER 1993–REVISED MARCH 2005

**DESCRIPTION/ORDERING INFORMATION (CONTINUED)**

Data on the A or B bus is clocked into the registers on the low-to-high transition of the appropriate clock (CLKAB or CLKBA) input. Figure 1 illustrates the four fundamental bus-management functions that can be performed with the SN74LVCH16646A.

Output-enable ( $\overline{OE}$ ) and direction-control (DIR) inputs control the transceiver functions. In the transceiver mode, data present at the high-impedance port can be stored in either register or in both. The select-control (SAB and SBA) inputs can multiplex stored and real-time (transparent mode) data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data. DIR determines which bus receives data when  $\overline{OE}$  is low. In the isolation mode ( $\overline{OE}$  high), A data can be stored in one register and/or B data can be stored in the other register.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

When an output function is disabled, the input function still is enabled and can be used to store and transmit data. Only one of the two buses, A or B, can be driven at a time.

Inputs can be driven from either 3.3-V or 5-V devices. This feature allows the use of this device as a translator in a mixed 3.3-V/5-V system environment.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

**FUNCTION TABLE**

| INPUTS          |     |        |        |     |     | DATA I/O <sup>(1)</sup> |             | OPERATION OR FUNCTION                 |
|-----------------|-----|--------|--------|-----|-----|-------------------------|-------------|---------------------------------------|
| $\overline{OE}$ | DIR | CLKAB  | CLKBA  | SAB | SBA | A1–A8                   | B1–B8       |                                       |
| X               | X   | ↑      | X      | X   | X   | Input                   | Unspecified | Store A, B unspecified <sup>(1)</sup> |
| X               | X   | X      | ↑      | X   | X   | Unspecified             | Input       | Store B, A unspecified <sup>(1)</sup> |
| H               | X   | ↑      | ↑      | X   | X   | Input                   | Input       | Store A and B data                    |
| H               | X   | H or L | H or L | X   | X   | Input                   | Input       | Isolation, hold storage               |
| L               | L   | X      | X      | X   | L   | Output                  | Input       | Real-time B data to A bus             |
| L               | L   | X      | H or L | X   | H   | Output                  | Input       | Stored B data to A bus                |
| L               | H   | X      | X      | L   | X   | Input                   | Output      | Real-time A data to B Bus             |
| L               | H   | H or L | X      | H   | X   | Input                   | Output      | Stored A data to bus                  |

(1) The data-output functions can be enabled or disabled by various signals at  $\overline{OE}$  or DIR. Data-input functions always are enabled, i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

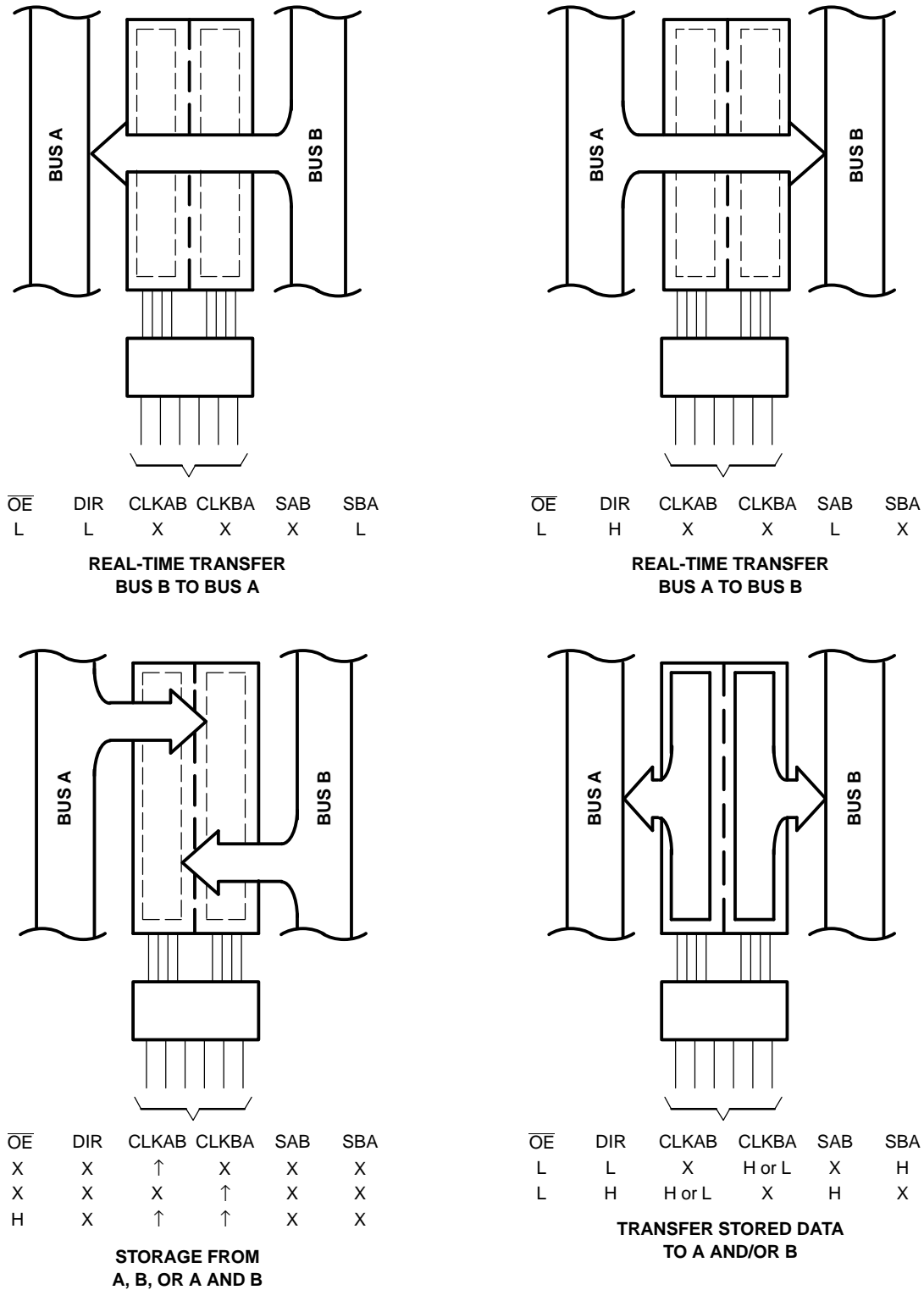
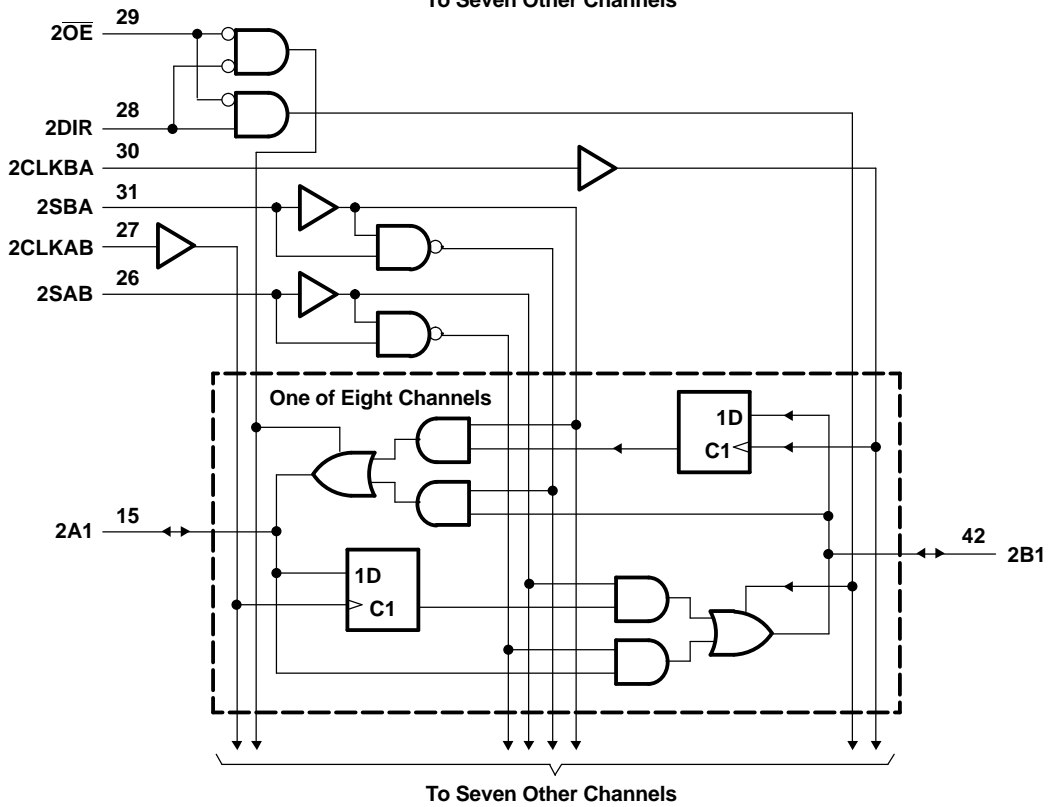
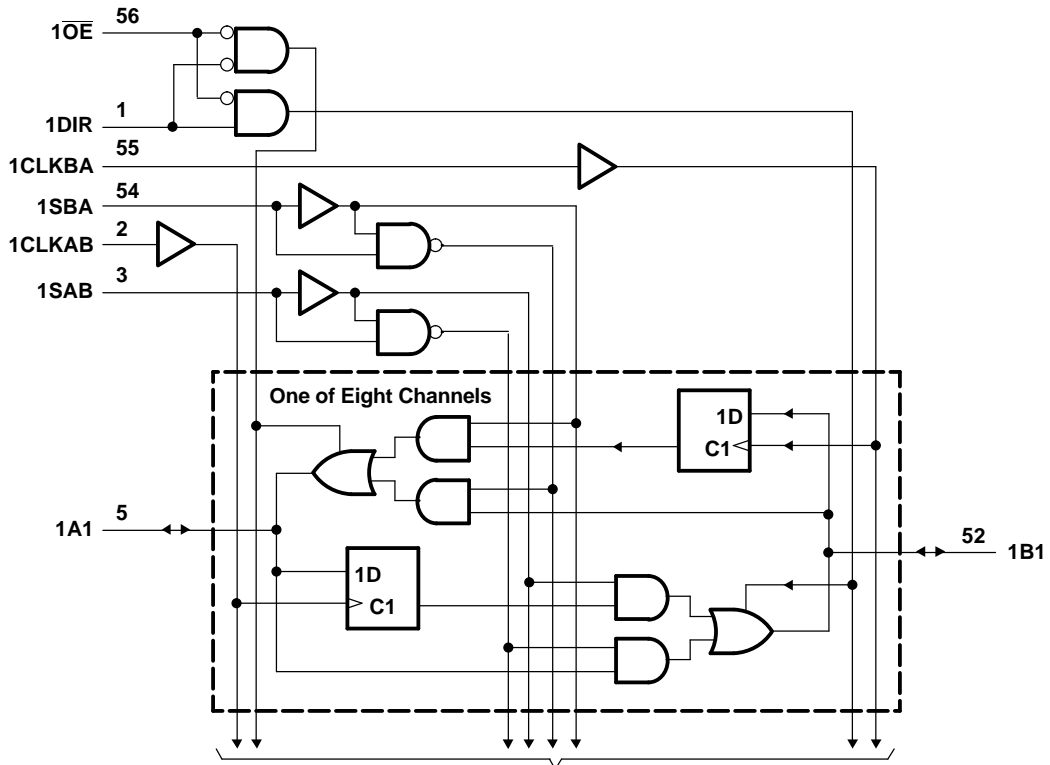


Figure 1. Bus-Management Functions

**SN74LVCH16646A**  
**16-BIT BUS TRANSCEIVER AND REGISTER**  
**WITH 3-STATE OUTPUTS**

SCAS318K—NOVEMBER 1993—REVISED MARCH 2005

**LOGIC DIAGRAM (POSITIVE LOGIC)**



**Absolute Maximum Ratings<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

|   |   | MIN         | MAX            | UNIT    |
|---|---|-------------|----------------|---------|
| $V_{CC}$  | Supply voltage range  | -0.5        | 6.5            | V       |
| $V_I$   | Input voltage range <sup>(2)</sup>  | -0.5        | 6.5            | V       |
| $V_O$   | Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup> | -0.5        | 6.5            | V       |
| $V_O$   | Voltage range applied to any output in the high or low state <sup>(2)(3)</sup>              | -0.5        | $V_{CC} + 0.5$ | V       |
| $I_{IK}$  | Input clamp current   | $V_I < 0$   |                | -50 mA  |
| $I_{OK}$  | Output clamp current  | $V_O < 0$   |                | -50 mA  |
| $I_O$   | Continuous output current   |             |                | ±50 mA  |
| Continuous current through each $V_{CC}$ or GND |   |             |                | ±100 mA |
| $\theta_{JA}$                                   | Package thermal impedance <sup>(4)</sup>  | DGG package |                | 64 °C/W |
|   |   | DGV package |                | 48      |
|   |   | DL package  |                | 56      |
| $T_{stg}$                                       | Storage temperature range   | -65         | 150            | °C      |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) The value of  $V_{CC}$  is provided in the recommended operating conditions table.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

**Recommended Operating Conditions<sup>(1)</sup>**

|                     |                                    | MIN                                       | MAX                  | UNIT     |    |
|---------------------|------------------------------------|---|----------------------|----------|----|
| $V_{CC}$            | Supply voltage                     | Operating                                 | 1.65                 | 3.6      | V  |
|                     |                                    | Data retention only                       | 1.5                  |          |    |
| $V_{IH}$            | High-level input voltage           | $V_{CC} = 1.65\text{ V to }1.95\text{ V}$ | $0.65 \times V_{CC}$ |          | V  |
|                     |                                    | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$   | 1.7                  |          |    |
|                     |                                    | $V_{CC} = 2.7\text{ V to }3.6\text{ V}$   | 2                    |          |    |
| $V_{IL}$            | Low-level input voltage            | $V_{CC} = 1.65\text{ V to }1.95\text{ V}$ | $0.35 \times V_{CC}$ |          | V  |
|                     |                                    | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$   | 0.7                  |          |    |
|                     |                                    | $V_{CC} = 2.7\text{ V to }3.6\text{ V}$   | 0.8                  |          |    |
| $V_I$               | Input voltage                      | 0   | 5.5                  | V        |    |
| $V_O$               | Output voltage                     | High or low state                         | 0                    | $V_{CC}$ | V  |
|                     |                                    | 3-state                                   | 0                    | 5.5      |    |
| $I_{OH}$            | High-level output current          | $V_{CC} = 1.65\text{ V}$                  |                      | -4       | mA |
|                     |                                    | $V_{CC} = 2.3\text{ V}$                   |                      | -8       |    |
|                     |                                    | $V_{CC} = 2.7\text{ V}$                   |                      | -12      |    |
|                     |                                    | $V_{CC} = 3\text{ V}$                     |                      | -24      |    |
| $I_{OL}$            | Low-level output current           | $V_{CC} = 1.65\text{ V}$                  |                      | 4        | mA |
|                     |                                    | $V_{CC} = 2.3\text{ V}$                   |                      | 8        |    |
|                     |                                    | $V_{CC} = 2.7\text{ V}$                   |                      | 12       |    |
|                     |                                    | $V_{CC} = 3\text{ V}$                     |                      | 24       |    |
| $\Delta t/\Delta v$ | Input transition rise or fall rate |   | 10                   | ns/V     |    |
| $T_A$               | Operating free-air temperature     | -40                                       | 85                   | °C       |    |

- (1) All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

# SN74LVCH16646A

## 16-BIT BUS TRANSCEIVER AND REGISTER WITH 3-STATE OUTPUTS

SCAS318K–NOVEMBER 1993–REVISED MARCH 2005

### Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                      |                          | TEST CONDITIONS  | V <sub>CC</sub> | MIN                   | TYP <sup>(1)</sup> | MAX  | UNIT |
|--------------------------------|--------------------------|--|-----------------|-----------------------|--------------------|------|------|
| V <sub>OH</sub>                |                          | I <sub>OH</sub> = –100 μA  | 1.65 V to 3.6 V | V <sub>CC</sub> – 0.2 |                    |      | V    |
|                                |                          | I <sub>OH</sub> = –4 mA  | 1.65 V          | 1.2                   |                    |      |      |
|                                |                          | I <sub>OH</sub> = –8 mA  | 2.3 V           | 1.7                   |                    |      |      |
|                                |                          | I <sub>OH</sub> = –12 mA   | 2.7 V           | 2.2                   |                    |      |      |
|                                |                          |  | 3 V             | 2.4                   |                    |      |      |
|                                | I <sub>OH</sub> = –24 mA | 3 V  | 2.2             |                       |                    |      |      |
| V <sub>OL</sub>                |                          | I <sub>OL</sub> = 100 μA   | 1.65 V to 3.6 V |                       |                    | 0.2  | V    |
|                                |                          | I <sub>OL</sub> = 4 mA   | 1.65 V          |                       |                    | 0.45 |      |
|                                |                          | I <sub>OL</sub> = 8 mA   | 2.3 V           |                       |                    | 0.7  |      |
|                                |                          | I <sub>OL</sub> = 12 mA  | 2.7 V           |                       |                    | 0.4  |      |
|                                |                          | I <sub>OL</sub> = 24 mA  | 3 V             |                       |                    | 0.55 |      |
| I <sub>I</sub>                 | Control inputs           | V <sub>I</sub> = 0 to 5.5 V  | 3.6 V           |                       |                    | ±5   | μA   |
| I <sub>I(hold)</sub>           | A or B ports             | V <sub>I</sub> = 0.58 V  | 1.65 V          | (2)                   |                    |      | μA   |
|                                |                          | V <sub>I</sub> = 1.07 V  |                 | (2)                   |                    |      |      |
|                                |                          | V <sub>I</sub> = 0.7 V   | 2.3 V           | 45                    |                    |      |      |
|                                |                          | V <sub>I</sub> = 1.7 V   |                 | –45                   |                    |      |      |
|                                |                          | V <sub>I</sub> = 0.8 V   | 3 V             | 75                    |                    |      |      |
|                                |                          | V <sub>I</sub> = 2 V   |                 | –75                   |                    |      |      |
|                                |                          | V <sub>I</sub> = 0 to 3.6 V <sup>(3)</sup>                                   | 3.6 V           | ±500                  |                    |      |      |
| I <sub>off</sub>               |                          | V <sub>I</sub> or V <sub>O</sub> = 5.5 V                                     | 0               |                       |                    | ±10  | μA   |
| I <sub>OZ</sub> <sup>(4)</sup> |                          | V <sub>O</sub> = 0 to 5.5 V  | 3.6 V           |                       |                    | ±10  | μA   |
| I <sub>CC</sub>                |                          | V <sub>I</sub> = V <sub>CC</sub> or GND                                      | 3.6 V           | I <sub>O</sub> = 0    |                    | 20   | μA   |
|                                |                          | 3.6 V ≤ V <sub>I</sub> ≤ 5.5 V <sup>(5)</sup>                                |                 |                       |                    | 20   |      |
| ΔI <sub>CC</sub>               |                          | One input at V <sub>CC</sub> – 0.6 V, Other inputs at V <sub>CC</sub> or GND | 2.7 V to 3.6 V  |                       |                    | 500  | μA   |
| C <sub>i</sub>                 | Control inputs           | V <sub>I</sub> = V <sub>CC</sub> or GND                                      | 3.3 V           |                       |                    | 5    | pF   |
| C <sub>io</sub>                | A or B ports             | V <sub>O</sub> = V <sub>CC</sub> or GND                                      | 3.3 V           |                       |                    | 8.5  | pF   |

(1) All typical values are at V<sub>CC</sub> = 3.3 V, T<sub>A</sub> = 25°C.

(2) This information was not available at the time of publication.

(3) This is the bus-hold maximum dynamic current required to switch the input from one state to another.

(4) For I/O ports, the parameter I<sub>OZ</sub> includes the input leakage current, but not I<sub>I(hold)</sub>.

(5) This applies in the disabled state only.

### Timing Requirements

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 2)

|                    |  | V <sub>CC</sub> = 1.8 V<br>± 0.15 V |     | V <sub>CC</sub> = 2.5 V<br>± 0.2 V |     | V <sub>CC</sub> = 2.7 V |     | V <sub>CC</sub> = 3.3 V<br>± 0.3 V |     | UNIT |
|--------------------|--|-------------------------------------|-----|------------------------------------|-----|-------------------------|-----|------------------------------------|-----|------|
|                    |  | MIN                                 | MAX | MIN                                | MAX | MIN                     | MAX | MIN                                | MAX |      |
| f <sub>clock</sub> | Clock frequency                            | (1)                                 |     | (1)                                |     | 150                     |     | 150                                |     | MHz  |
| t <sub>w</sub>     | Pulse duration, CLK high or low            | (1)                                 |     | (1)                                |     | 3.3                     |     | 3.3                                |     | ns   |
| t <sub>su</sub>    | Setup time, A or B before CLKAB↑ or CLKBA↑ | (1)                                 |     | (1)                                |     | 3.2                     |     | 2.9                                |     | ns   |
| t <sub>h</sub>     | Hold time, A or B after CLKAB↑ or CLKBA↑   | (1)                                 |     | (1)                                |     | 0                       |     | 0.3                                |     | ns   |

(1) This information was not available at the time of publication.

## Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 2)

| PARAMETER | FROM<br>(INPUT) | TO<br>(OUTPUT) | $V_{CC} = 1.8\text{ V} \pm 0.15\text{ V}$ |     | $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ |     | $V_{CC} = 2.7\text{ V}$ |     | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ |     | UNIT |
|-----------|-----------------|----------------|---|-----|--|-----|-------------------------|-----|--|-----|------|
|           |                 |                | MIN                                       | MAX | MIN                                      | MAX | MIN                     | MAX | MIN                                      | MAX |      |
| $f_{max}$ |                 |                | (1)                                       |     | (1)                                      |     | 150                     |     | 150                                      |     | MHz  |
| $t_{pd}$  | A or B          | B or A         | (1)                                       | (1) | (1)                                      | (1) | 6.8                     |     | 1.3                                      | 5.7 | ns   |
|           | CLKAB or CLKBA  | A or B         | (1)                                       | (1) | (1)                                      | (1) | 7.9                     |     | 1.8                                      | 6.7 |      |
|           | SAB or SBA      |                | (1)                                       | (1) | (1)                                      | (1) | 9.2                     |     | 1.7                                      | 7.7 |      |
| $t_{en}$  | $\overline{OE}$ | A or B         | (1)                                       | (1) | (1)                                      | (1) | 8.5                     |     | 1.3                                      | 6.9 | ns   |
| $t_{dis}$ |                 |                | (1)                                       | (1) | (1)                                      | (1) | 7.7                     |     | 2.1                                      | 6.9 |      |
| $t_{en}$  | DIR             | A or B         | (1)                                       | (1) | (1)                                      | (1) | 8.5                     |     | 1.4                                      | 7.2 | ns   |
| $t_{dis}$ |                 |                | (1)                                       | (1) | (1)                                      | (1) | 7.8                     |     | 2  | 7   |      |

(1) This information was not available at the time of publication.

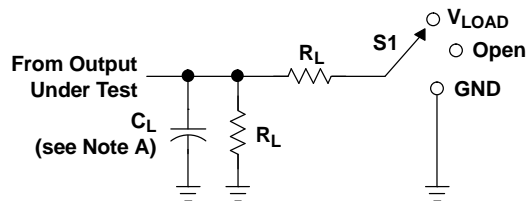
## Operating Characteristics

$T_A = 25^\circ\text{C}$

| PARAMETER |   | TEST<br>CONDITIONS | $V_{CC} = 1.8\text{ V}$ | $V_{CC} = 2.5\text{ V}$ | $V_{CC} = 3.3\text{ V}$ | UNIT |
|-----------|---|--------------------|-------------------------|-------------------------|-------------------------|------|
|           |   |                    | TYP                     | TYP                     | TYP                     |      |
| $C_{pd}$  | Power dissipation capacitance per transceiver | Outputs enabled    | (1)                     | (1)                     | 60                      | pF   |
|           |   | Outputs disabled   | (1)                     | (1)                     | 12                      |      |

(1) This information was not available at the time of publication.

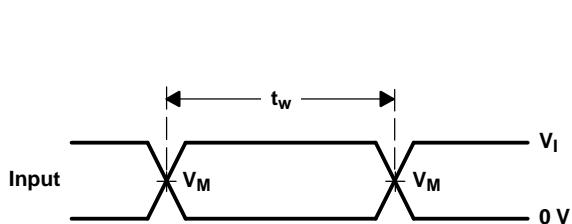
PARAMETER MEASUREMENT INFORMATION



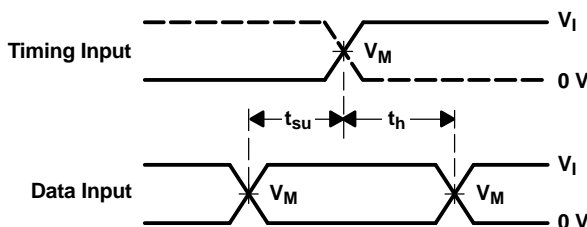
LOAD CIRCUIT

| TEST              | S1         |
|-------------------|------------|
| $t_{PLH}/t_{PHL}$ | Open       |
| $t_{PLZ}/t_{PZL}$ | $V_{LOAD}$ |
| $t_{PHZ}/t_{PZH}$ | GND        |

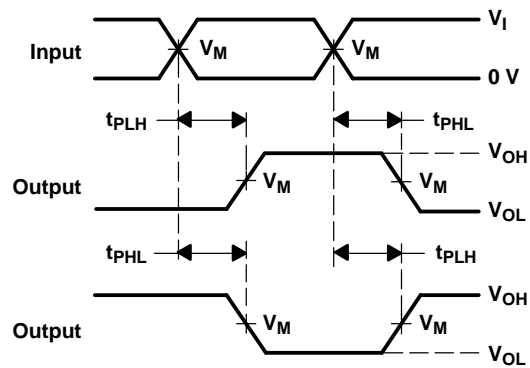
| $V_{CC}$                         | INPUTS   |                      | $V_M$      | $V_{LOAD}$        | $C_L$ | $R_L$        | $V_{\Delta}$ |
|----------------------------------|----------|----------------------|------------|-------------------|-------|--------------|--------------|
|                                  | $V_I$    | $t_r/t_f$            |            |                   |       |              |              |
| $1.8\text{ V} \pm 0.15\text{ V}$ | $V_{CC}$ | $\leq 2\text{ ns}$   | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 1 k $\Omega$ | 0.15 V       |
| $2.5\text{ V} \pm 0.2\text{ V}$  | $V_{CC}$ | $\leq 2\text{ ns}$   | $V_{CC}/2$ | $2 \times V_{CC}$ | 30 pF | 500 $\Omega$ | 0.15 V       |
| 2.7 V                            | 2.7 V    | $\leq 2.5\text{ ns}$ | 1.5 V      | 6 V               | 50 pF | 500 $\Omega$ | 0.3 V        |
| $3.3\text{ V} \pm 0.3\text{ V}$  | 2.7 V    | $\leq 2.5\text{ ns}$ | 1.5 V      | 6 V               | 50 pF | 500 $\Omega$ | 0.3 V        |



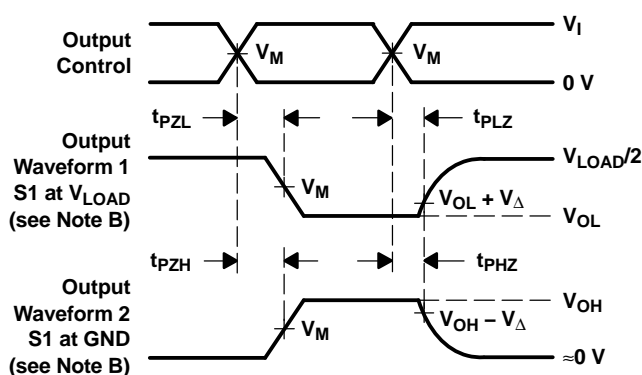
VOLTAGE WAVEFORMS  
PULSE DURATION



VOLTAGE WAVEFORMS  
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS  
PROPAGATION DELAY TIMES  
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS  
ENABLE AND DISABLE TIMES  
LOW- AND HIGH-LEVEL ENABLING

- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_O = 50\ \Omega$ .  
 D. The outputs are measured one at a time, with one transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .  
 H. All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms



**PACKAGING INFORMATION**

| Orderable Device   | Status <sup>(1)</sup> | Package Type | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup> | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|--------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| 74LVCH16646ADGGRE4 | ACTIVE                | TSSOP        | DGG             | 56   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| 74LVCH16646ADGGRG4 | ACTIVE                | TSSOP        | DGG             | 56   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| 74LVCH16646ADGVRE4 | ACTIVE                | TVSOP        | DGV             | 56   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| 74LVCH16646ADGVRG4 | ACTIVE                | TVSOP        | DGV             | 56   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| 74LVCH16646ADLRG4  | ACTIVE                | SSOP         | DL              | 56   | 1000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74LVCH16646ADGGR | ACTIVE                | TSSOP        | DGG             | 56   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74LVCH16646ADGVR | ACTIVE                | TVSOP        | DGV             | 56   | 2000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74LVCH16646ADL   | ACTIVE                | SSOP         | DL              | 56   | 20          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74LVCH16646ADLG4 | ACTIVE                | SSOP         | DL              | 56   | 20          | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74LVCH16646ADLR  | ACTIVE                | SSOP         | DL              | 56   | 1000        | Green (RoHS & no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

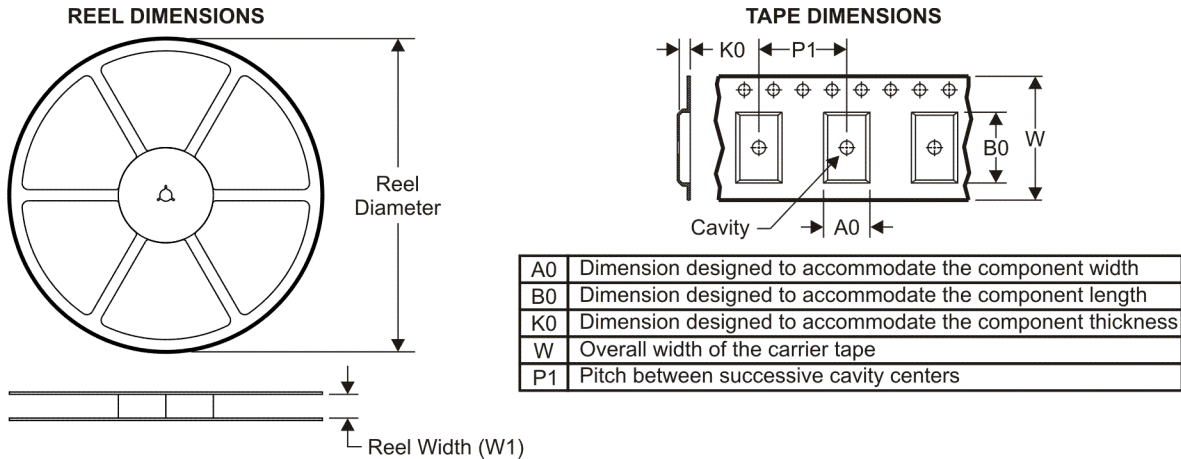
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

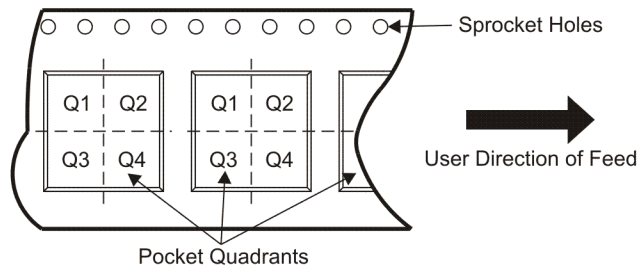
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**TAPE AND REEL INFORMATION**



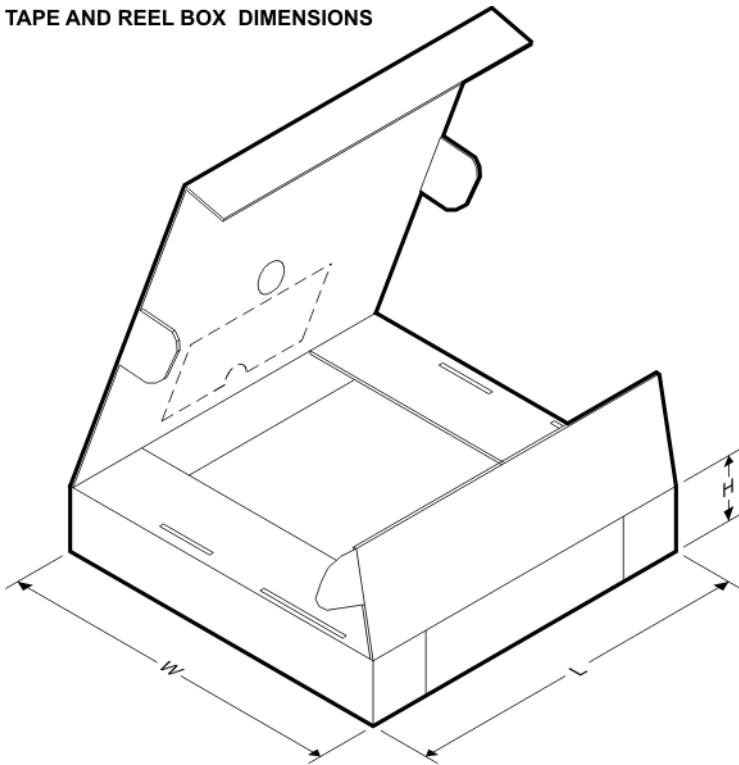
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



\*All dimensions are nominal

| Device             | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74LVCH16646ADGGR | TSSOP        | DGG             | 56   | 2000 | 330.0              | 24.4               | 8.6     | 15.6    | 1.8     | 12.0    | 24.0   | Q1            |
| SN74LVCH16646ADGVR | TVSOP        | DGV             | 56   | 2000 | 330.0              | 24.4               | 6.8     | 11.7    | 1.6     | 12.0    | 24.0   | Q1            |
| SN74LVCH16646ADLR  | SSOP         | DL              | 56   | 1000 | 330.0              | 32.4               | 11.35   | 18.67   | 3.1     | 16.0    | 32.0   | Q1            |

**TAPE AND REEL BOX DIMENSIONS**



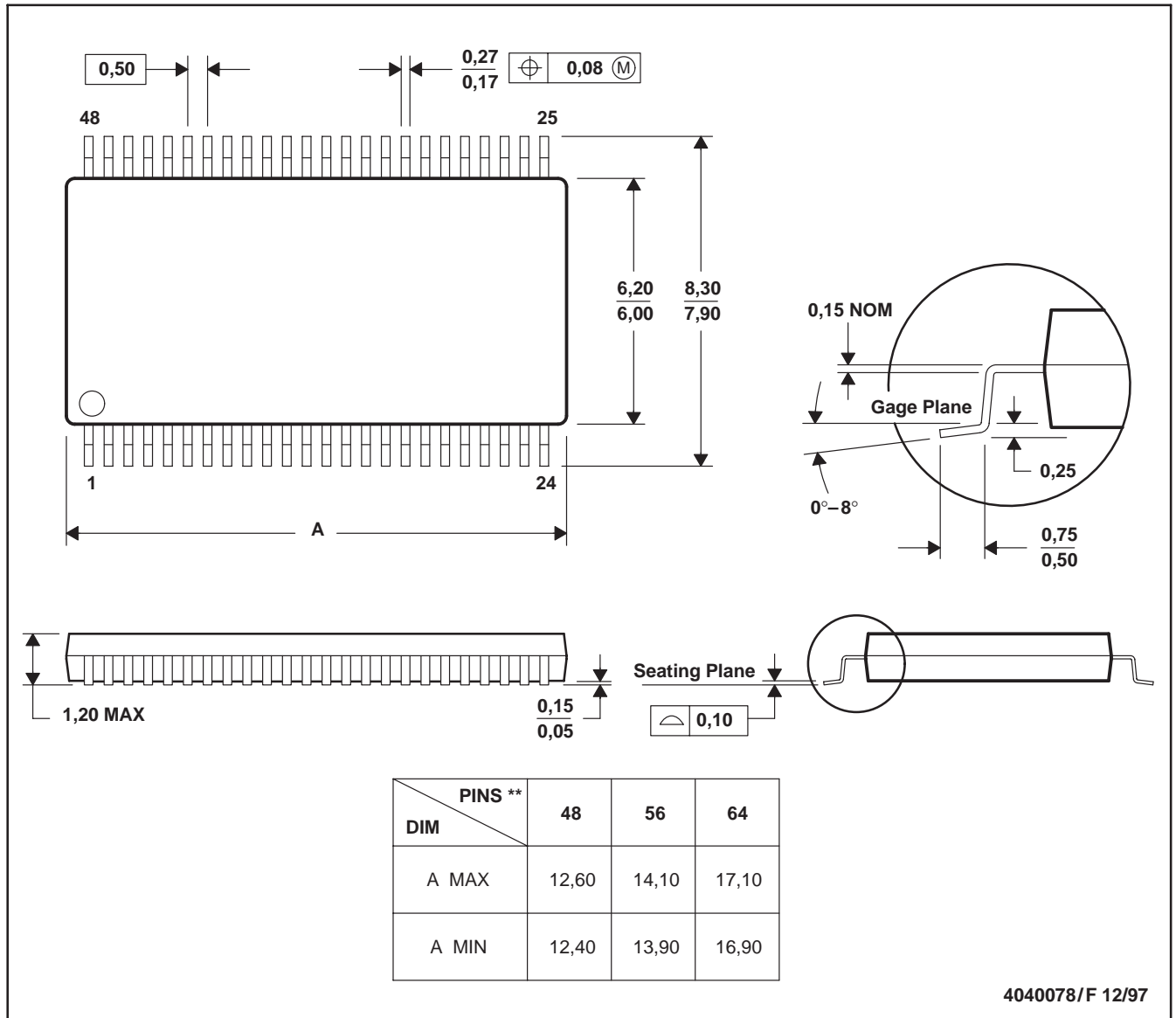
\*All dimensions are nominal

| Device             | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74LVCH16646ADGGR | TSSOP        | DGG             | 56   | 2000 | 346.0       | 346.0      | 41.0        |
| SN74LVCH16646ADGVR | TVSOP        | DGV             | 56   | 2000 | 346.0       | 346.0      | 41.0        |
| SN74LVCH16646ADLR  | SSOP         | DL              | 56   | 1000 | 346.0       | 346.0      | 49.0        |

DGG (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

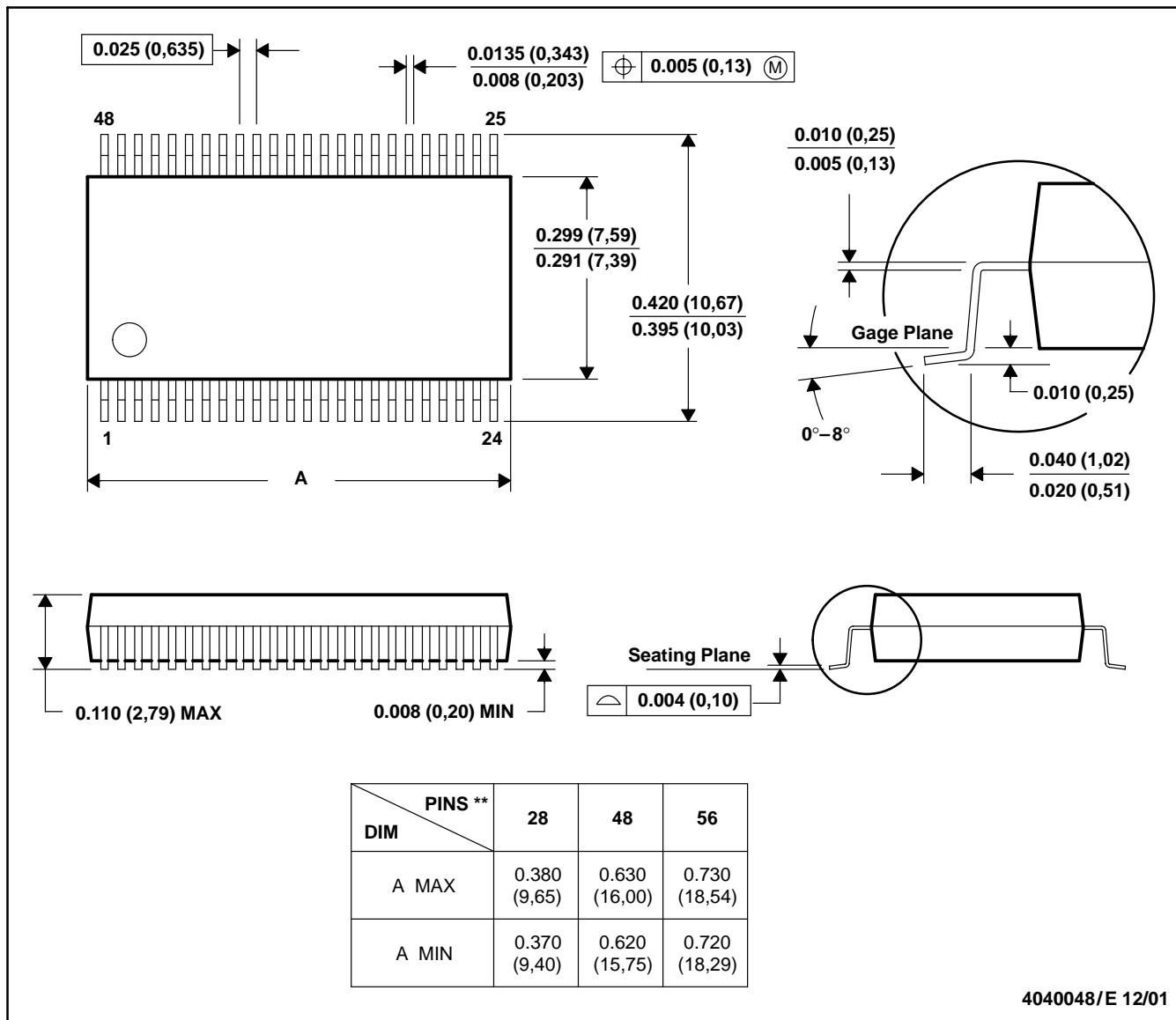


- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

DL (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

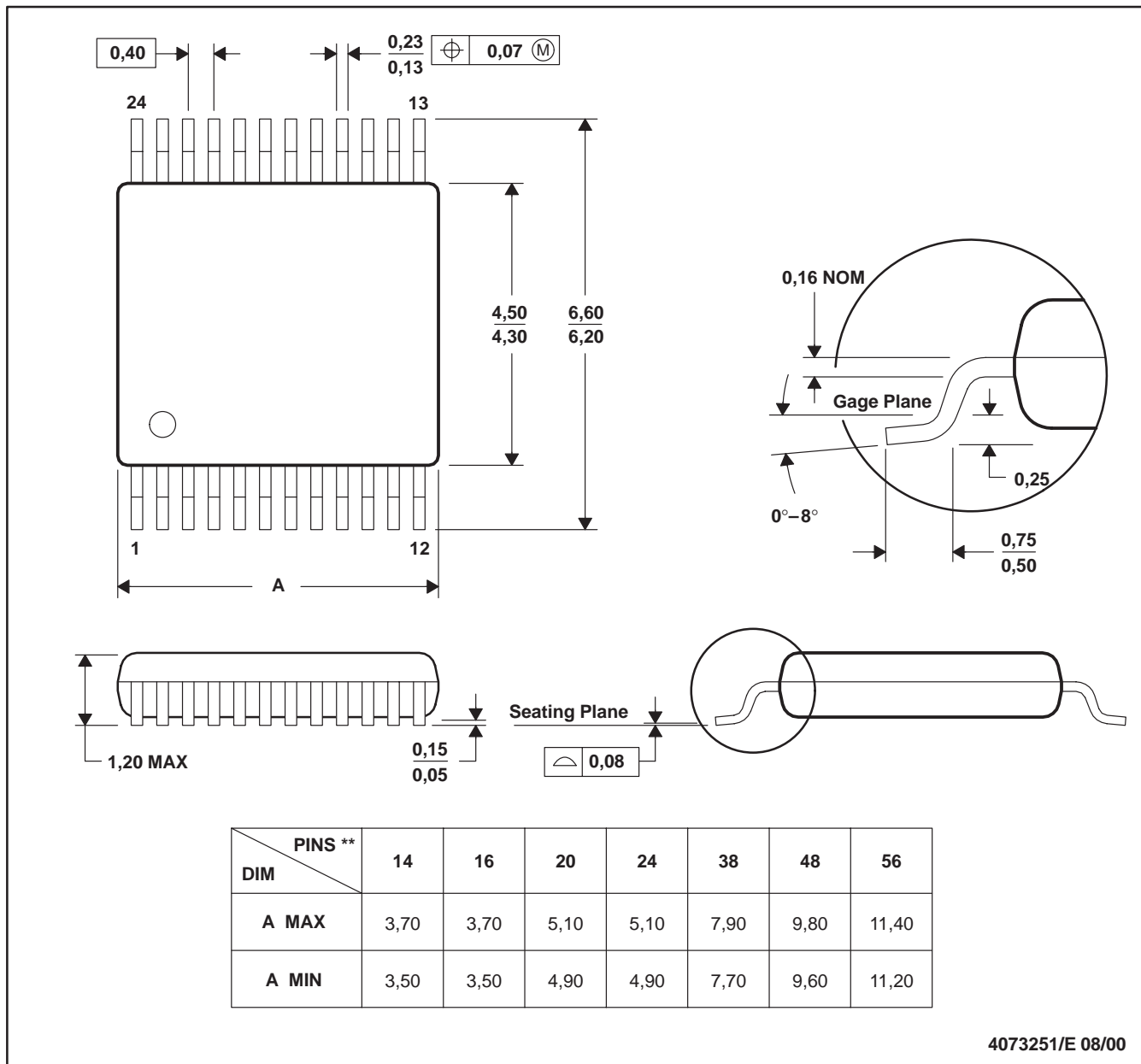


- NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).  
 D. Falls within JEDEC MO-118

DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

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